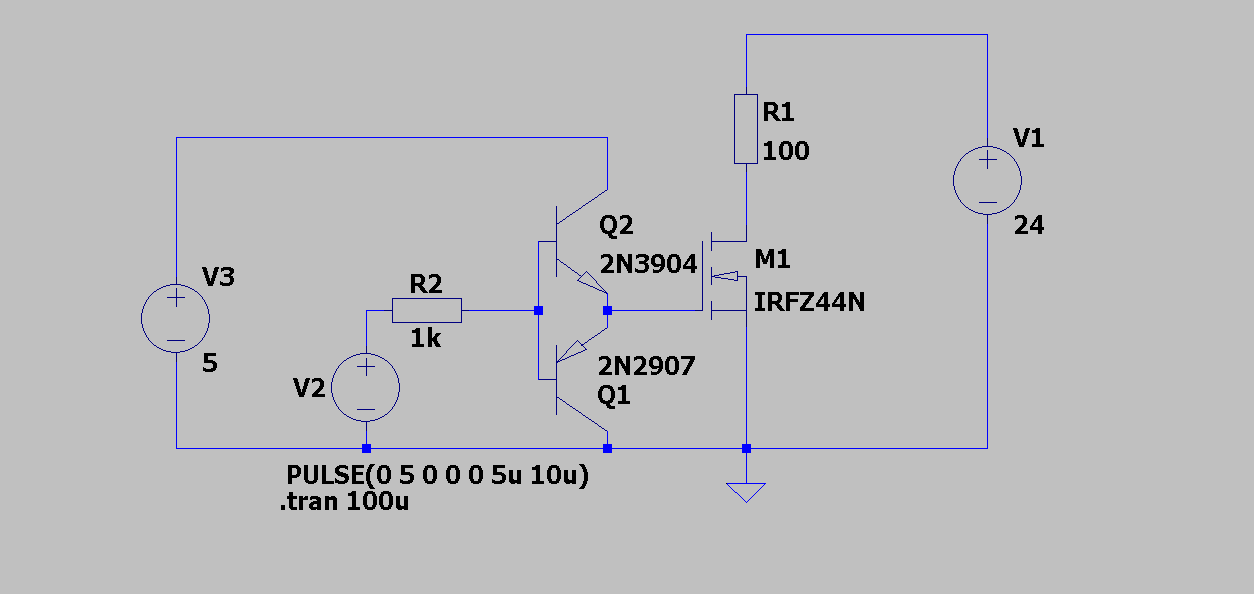
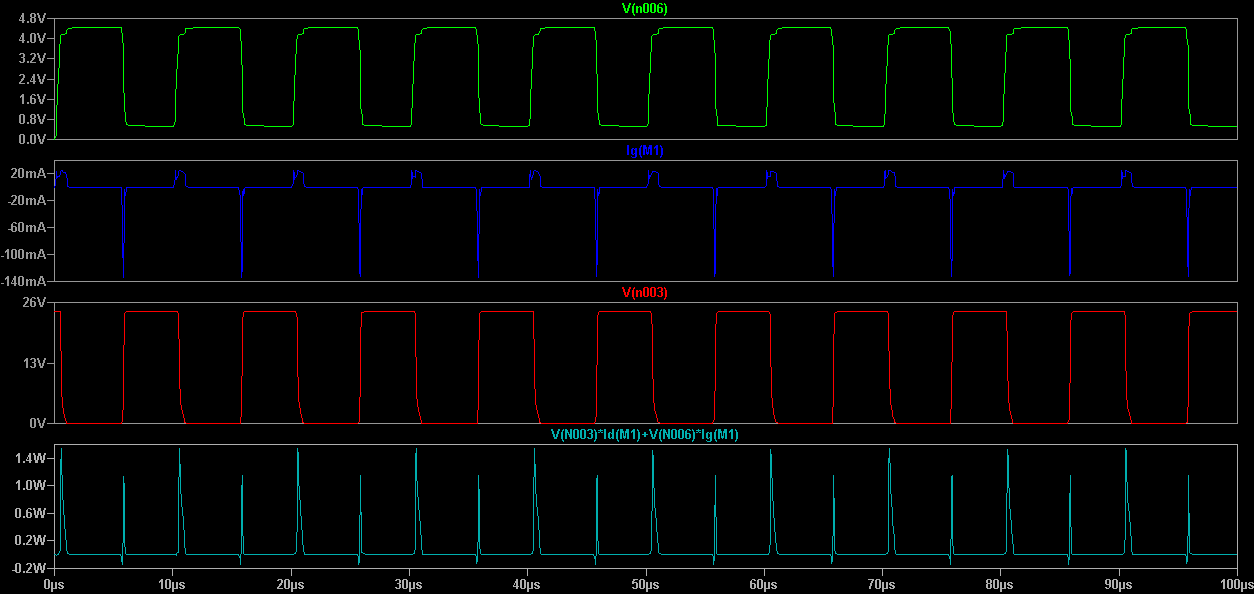
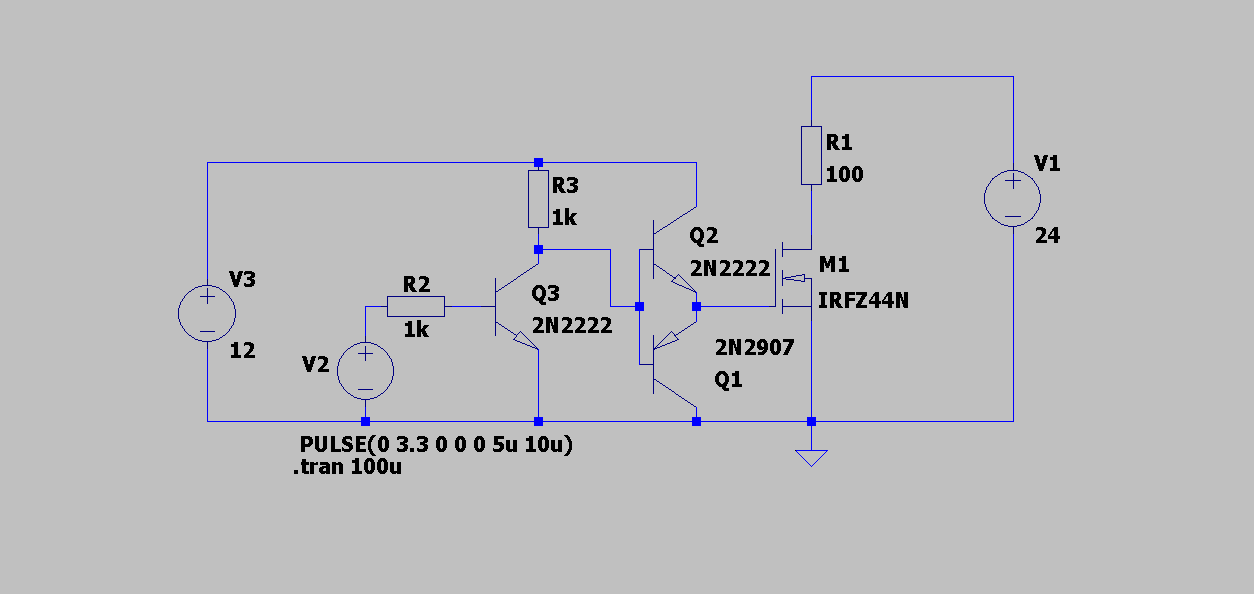
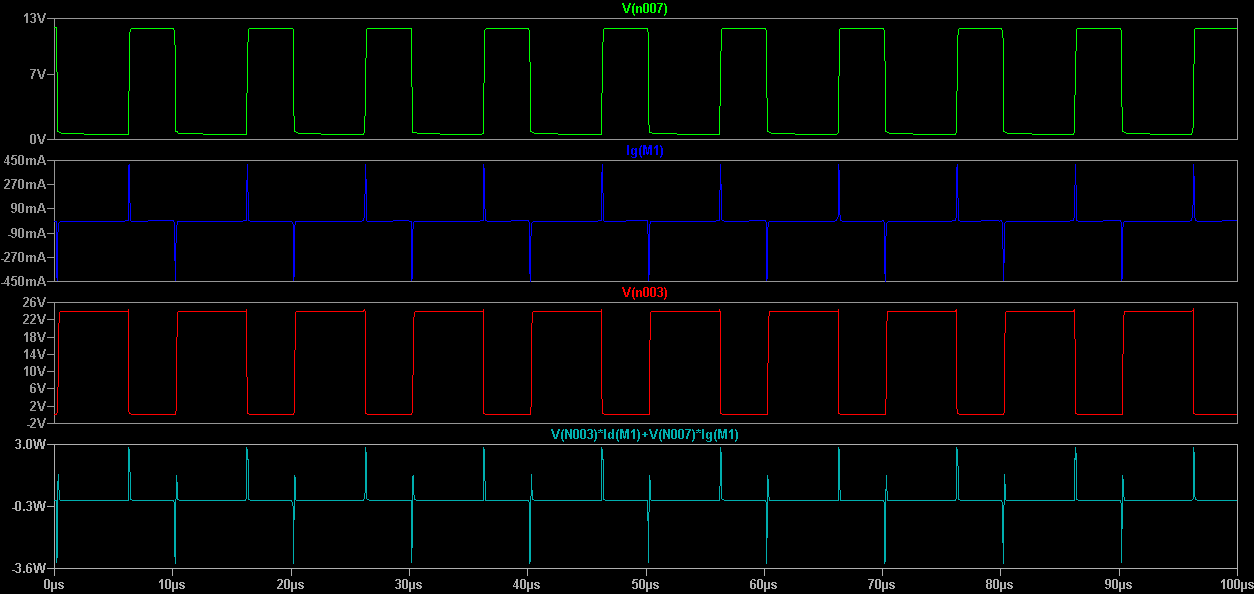
Circuit 2:





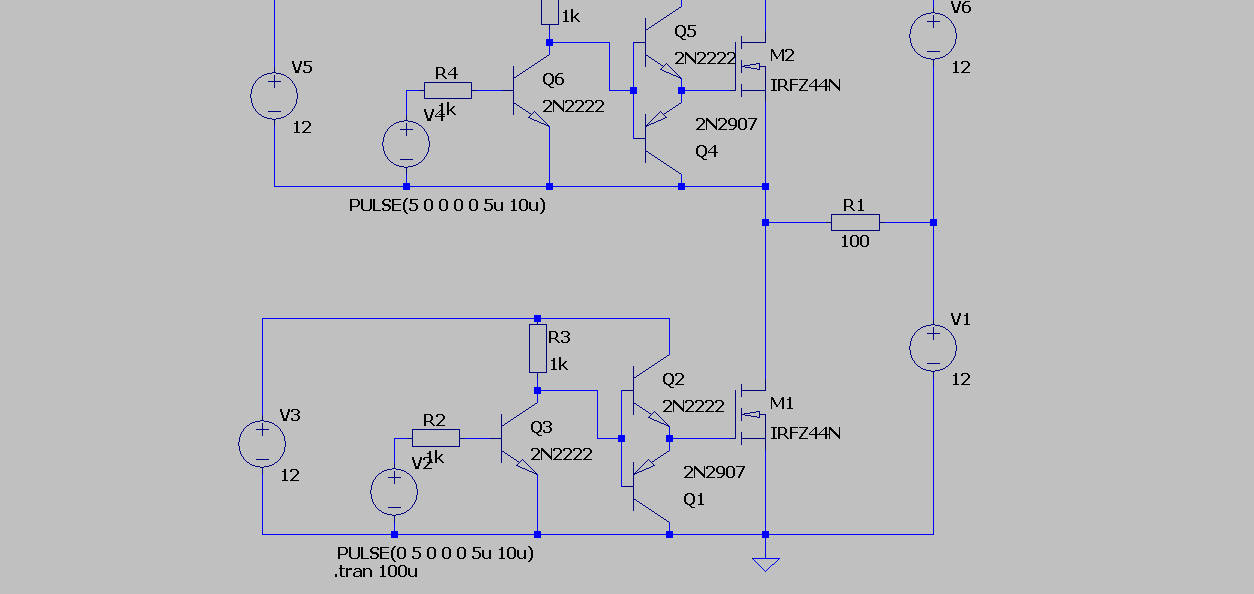
Circuit 3:





Circuit 4:

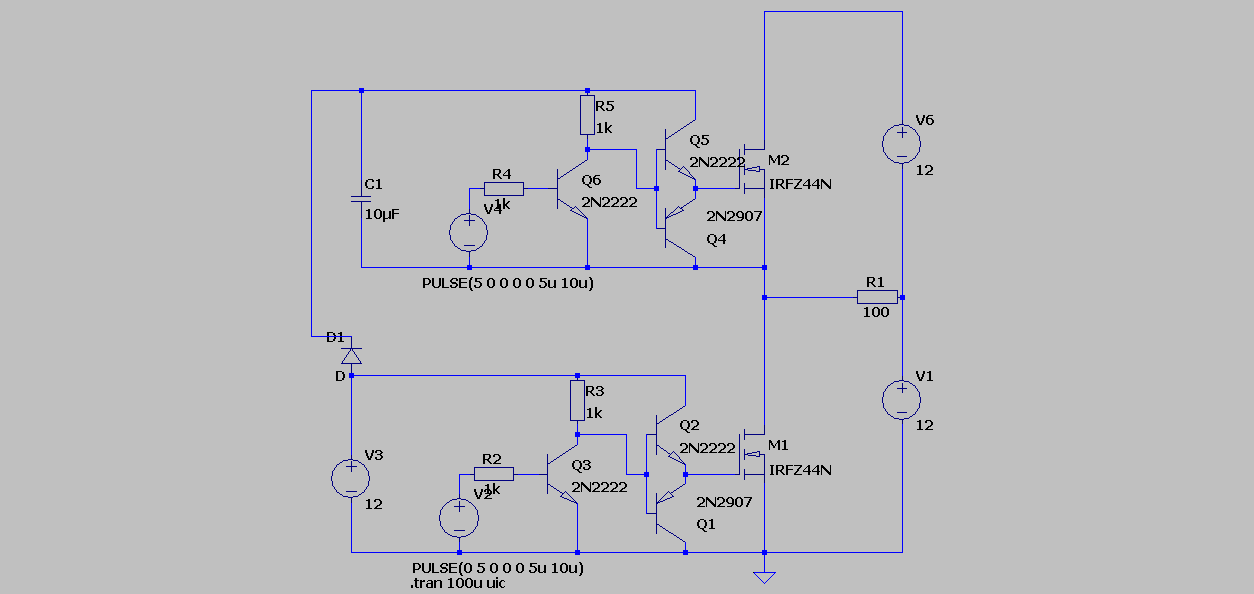
Circuit 4 includes two copies of the drive circuit from Circuit3 to allow upper and lower MOSFETS in a half bridge to be driven. Plot the voltage across R1 (not the voltage with respect to ground). Show that the voltage on the emitter of Q6 is very different to the voltage on the emitter of Q3 and hence rules out the possibility of the gate drives sharing a common ground.





Circuit 5:

Circuit 5 is a refinement of Circuit 4. It allows us to eliminate the power source for the upper gate drive – how is this achieved? How does the size of C1 affect the performance of the circuit (i.e. if it is made MUCH larger or MUCH smaller)



Circuit 6:

Circuit 6 derives the signal for the upper transistor from the lower signal. Draw up a table showing the on/off state for all transistors in the circuit when the input is high and low. Plot the drain current of M2 – why is it showing such huge peaks?

Circuit 7:

Circuit 7 is a commercial high/low side gate driver. Compare its performance with circuit 6 in the following areas: shoot-through (better? If so how is this achieved) input – output delay for rising and falling edges.

Additional task: Identify a high/low gate drive IC such as the one in Circuit 7 which also includes over current protection.